Intel Xeon E5 v2 Architecture

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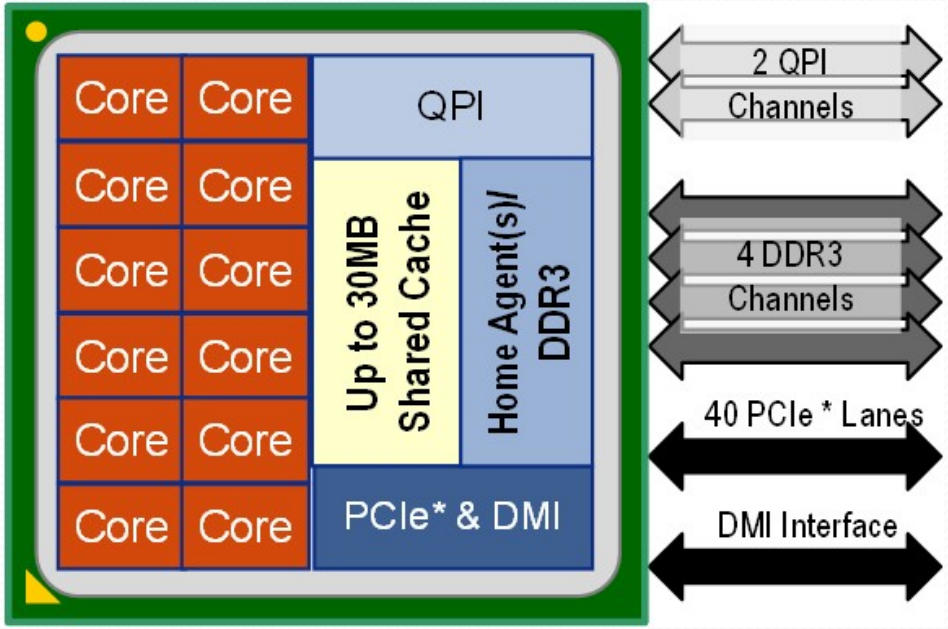
Xeon E5 v2

- General Overview
- Memory
- Ring Interconnect
- I/O
- Pipeline
- Intel AVX
- Security
- Benchmarks
- Applications

General Overview

- Ivy Bridge-E
- 2600v2 series
- 2.4 GHz clock, 3.4 GHz Turbo
- Tray Price: $2366.00
- LGA 2011 Socket
- ISA: Intel 64
- 12 Cores/24 Threads
- No integrated GPU

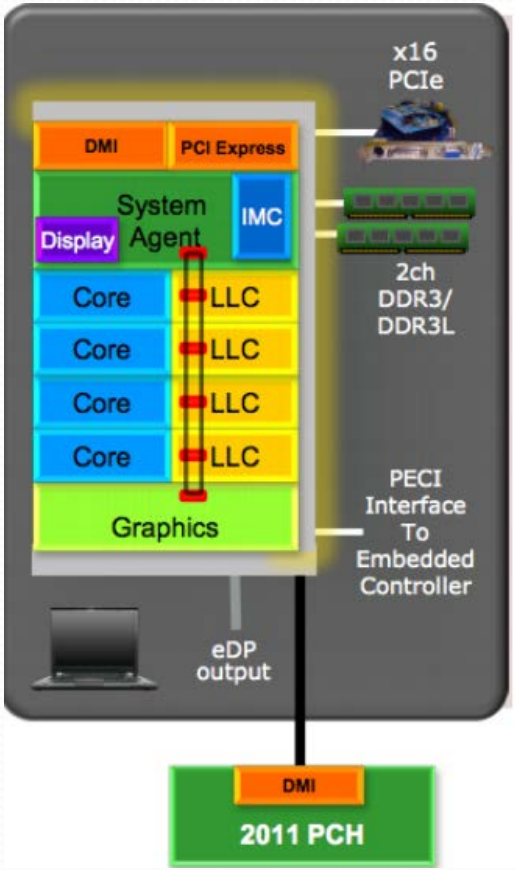


Memory

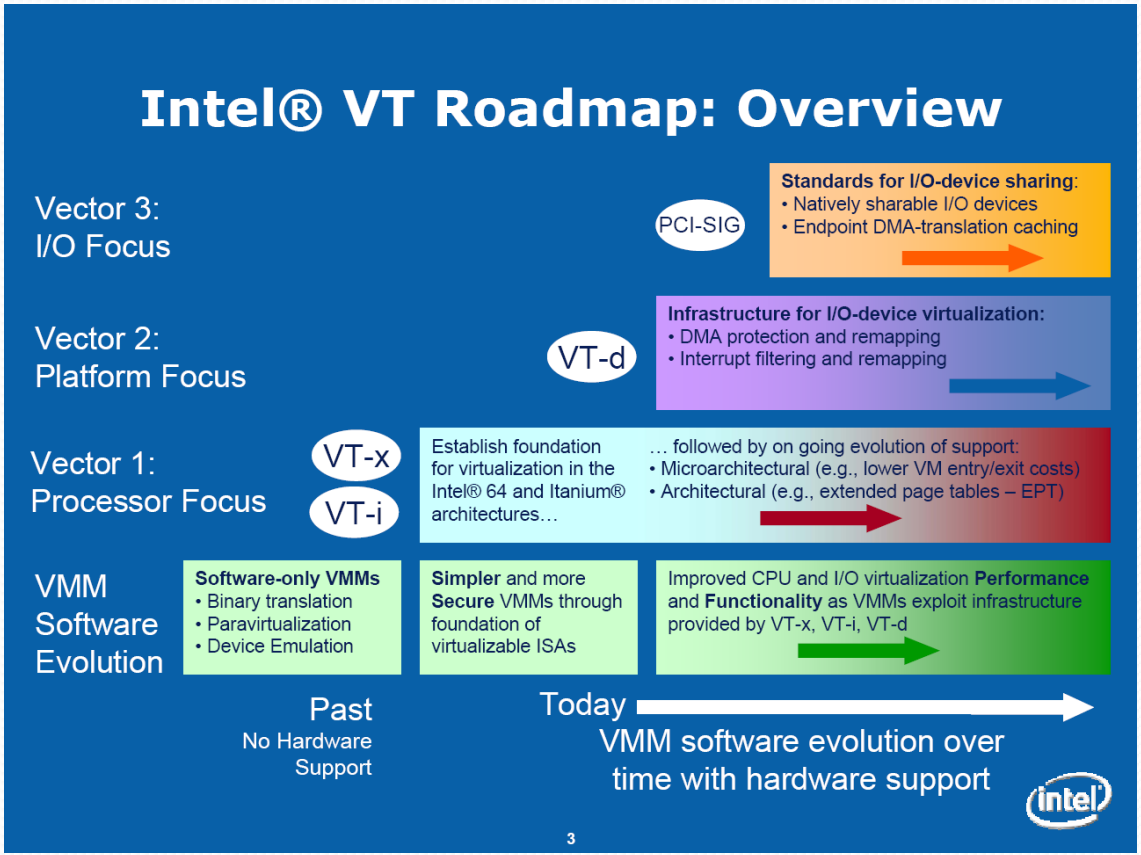
- Supports up to 768GB DDR3
- 46-bit addressing, 48-bit virtual addressing
- 3 levels of cache
- 4 memory channels
- 1 GB page support for server applications

Ring Interconnect

- Connects all components which require access to memory.
- Data ring is 32-bytes
- Request Ring
- ACK Ring
- Snoop Ring



I/O - Intel VT


Intel® VT Roadmap: Overview
Vector 3:
I/O Focus
PCI-SIG
Standards for I/O-device sharing:
• Natively sharable I/O devices
• Endpoint DMA-translation caching
Vector 2:
Platform Focus
VT-d
Infrastructure for I/O-device virtualization:
• DMA protection and remapping
• Interrupt filtering and remapping
Vector 1:
Processor Focus
VT-x
VT-i
Establish foundation for virtualization in the Intel® 64 and Itanium® architectures…
… followed by on going evolution of support:
• Microarchitectural (e.g., lower VM entry/exit costs)
• Architectural (e.g., extended page tables – EPT)
VMM
Software
Evolution
Software-only VMMs
• Binary translation
• Paravirtualization
• Device Emulation
Simpler and more Secure VMMs through foundation of virtualizable ISAs
Improved CPU and I/O virtualization Performance and Functionality as VMMs exploit infrastructure provided by VT-x, VT-i, VT-d
Past
No Hardware Support
Today
VMM software evolution over time with hardware support
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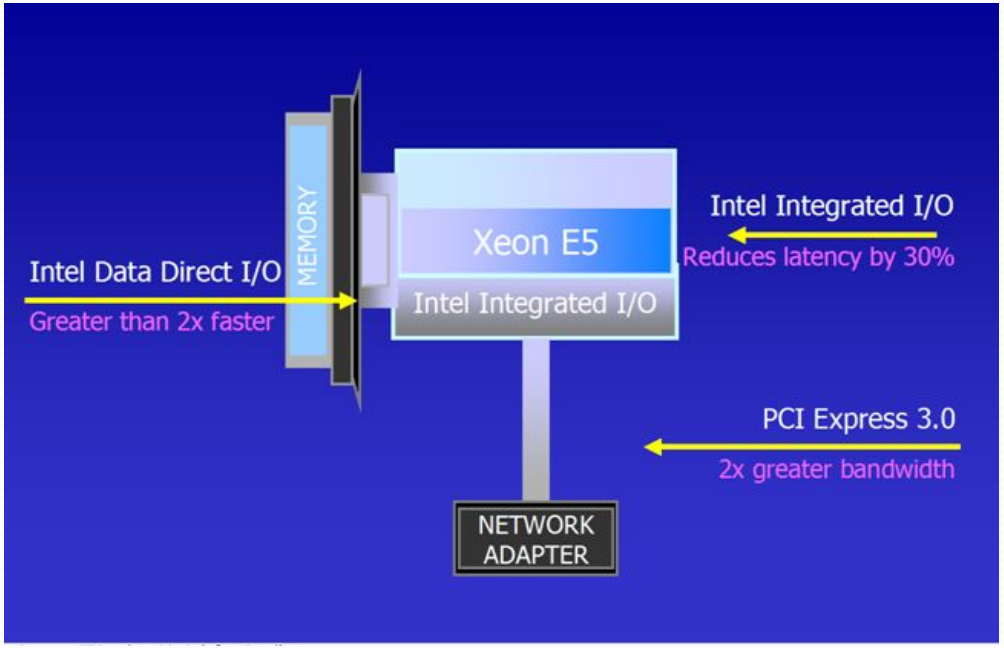
Intel Integrated I/O

- Introduced for Xeon E5 processors
- Removes memory bandwidth constraints
- Used with Ethernet controllers
- PCIe interface is integrated onto the processor itself, instead of an I/O hub or south bridge.



Pipeline

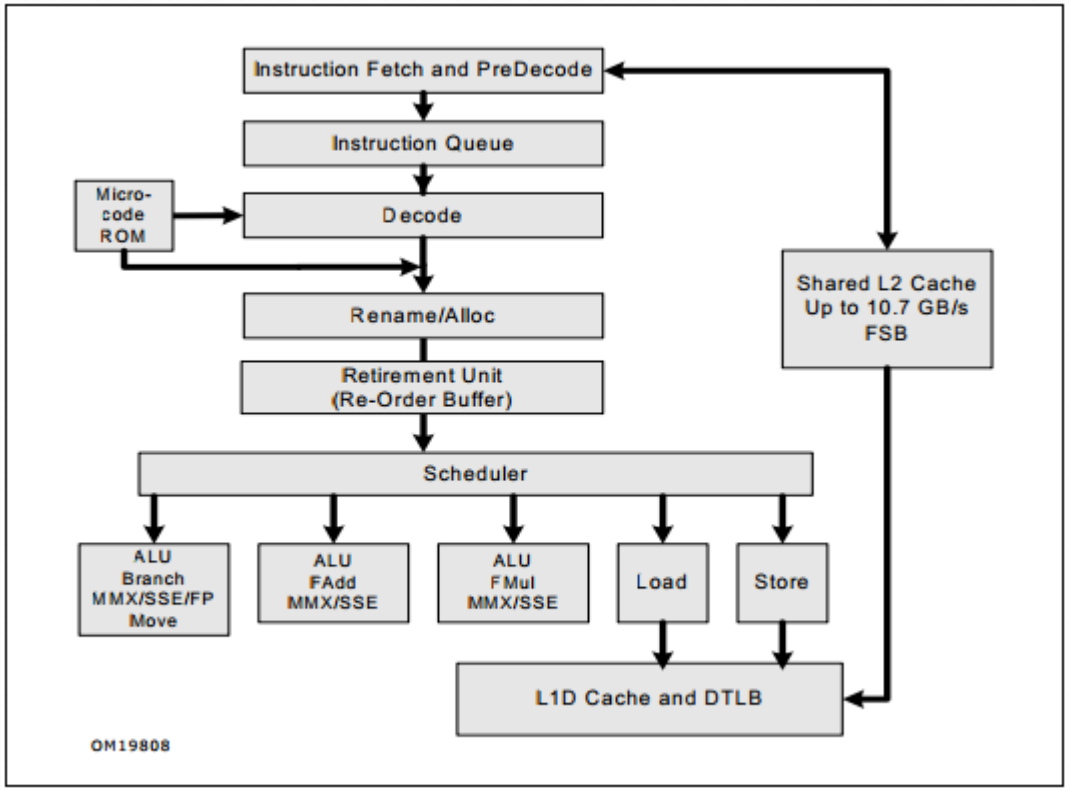
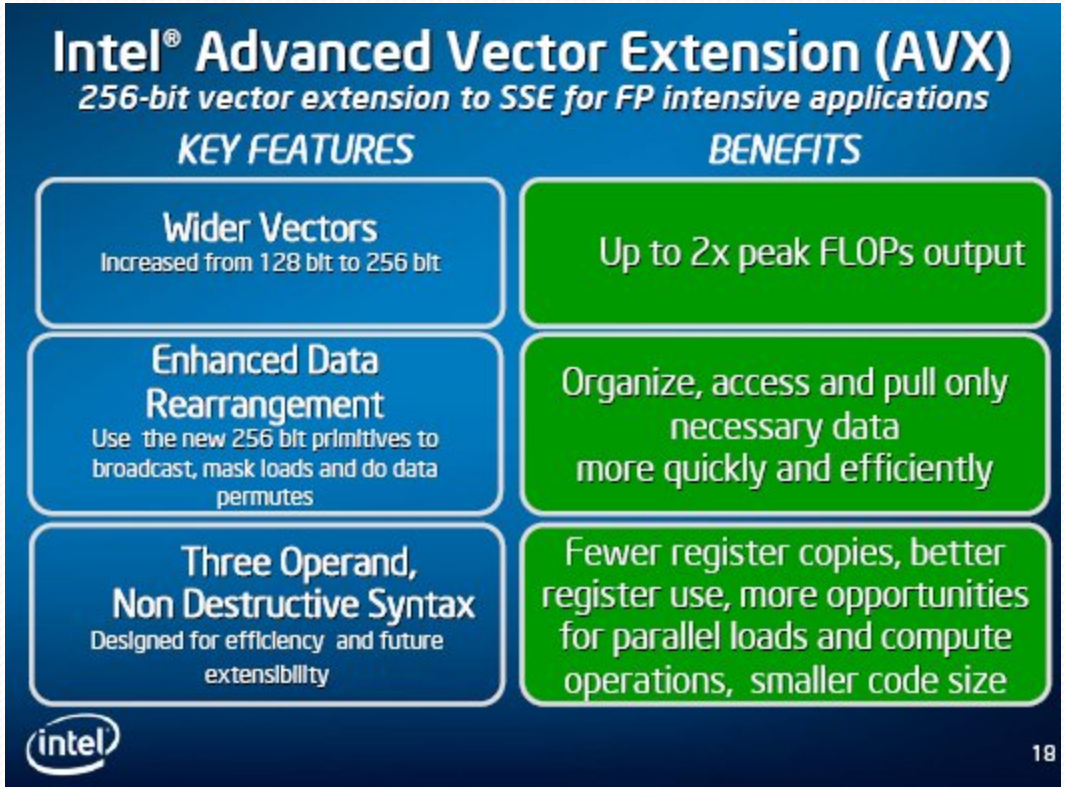


Figure 2-4. Intel Core Microarchitecture Pipeline Functionality

Intel AVX


Intel® Advanced Vector Extension (AVX)
256-bit vector extension to SSE for FP intensive applications
KEY FEATURES
BENEFITS
Wider Vectors
Increased from 128 bit to 256 bit
Up to 2x peak FLOPs output
Enhanced Data Rearrangement
Use the new 256 bit primitives to broadcast, mask loads and do data permutes
Organize, access and pull only necessary data more quickly and efficiently
Three Operand, Non Destructive Syntax
Designed for efficiency and future extensibility
Fewer register copies, better register use, more opportunities for parallel loads and compute operations, smaller code size
intel
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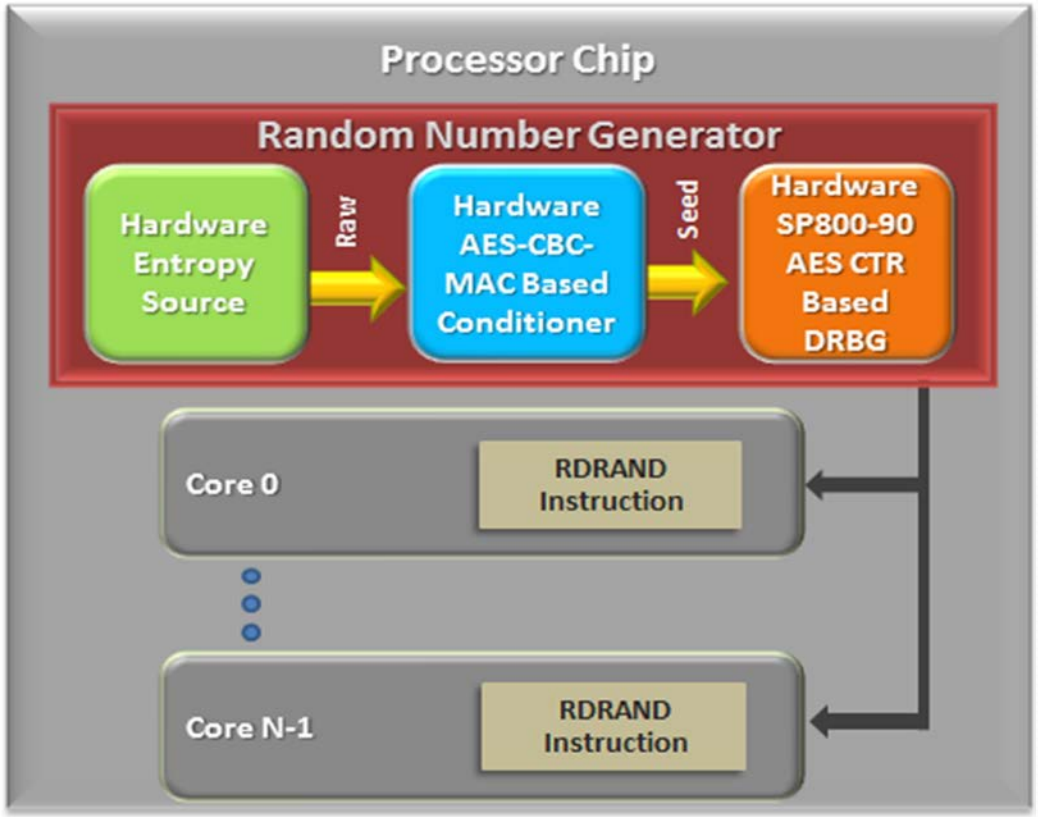
AES New Instructions

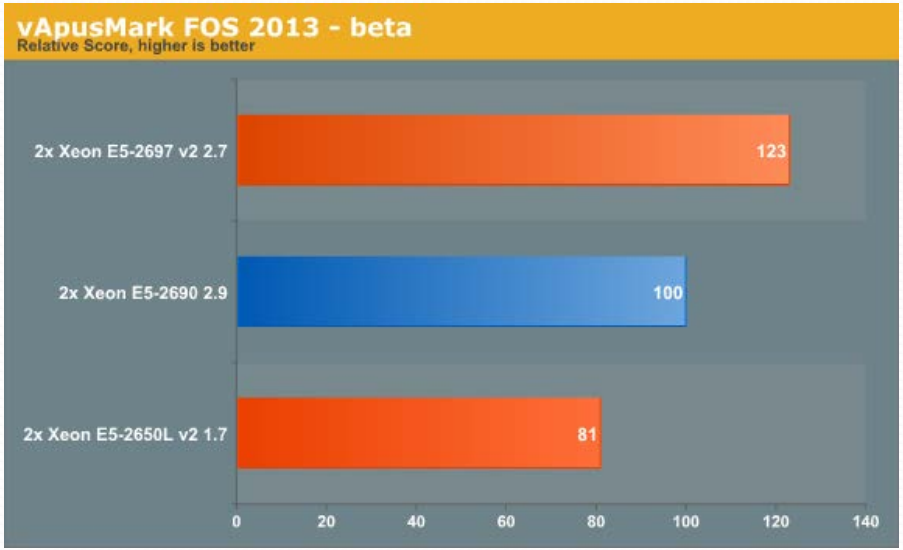
- Enables fast and secure data encryption and decryption.
- 6 Instructions offer full hardware support for AES
- 4 instructions for encryption and decryption
- 2 instructions for AES key expansion

Secure Key

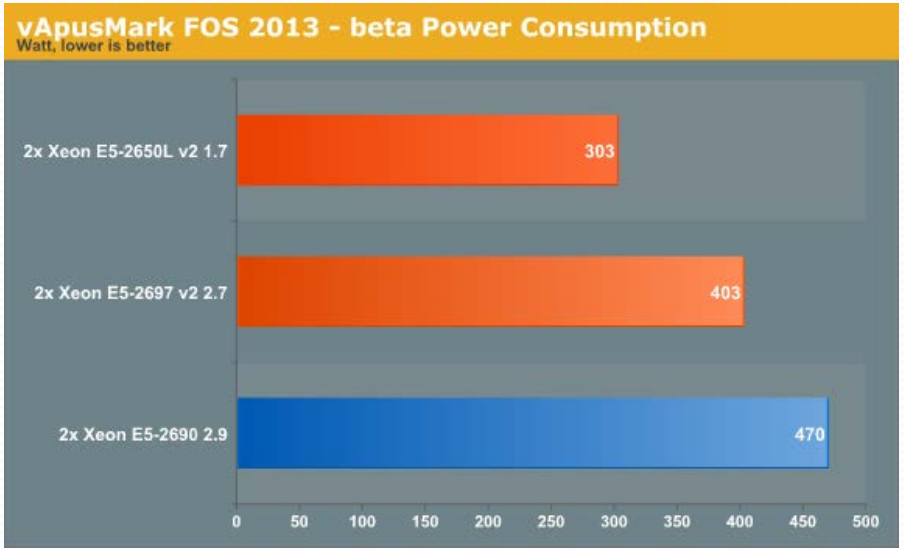

Processor Chip
Random Number Generator
Hardware Entropy Source
Raw
Hardware AES-CBC-MAC Based Conditioner
Seed
Hardware SP800-90 AES CTR Based DRBG
Core 0
RDRAND Instruction
Core N-1
RDRAND Instruction

Performance/Benchmarks

Sandy Bridge (2690) and Ivy Bridge (2679 v2) Comparison



Computation



Power Consumption

Applications

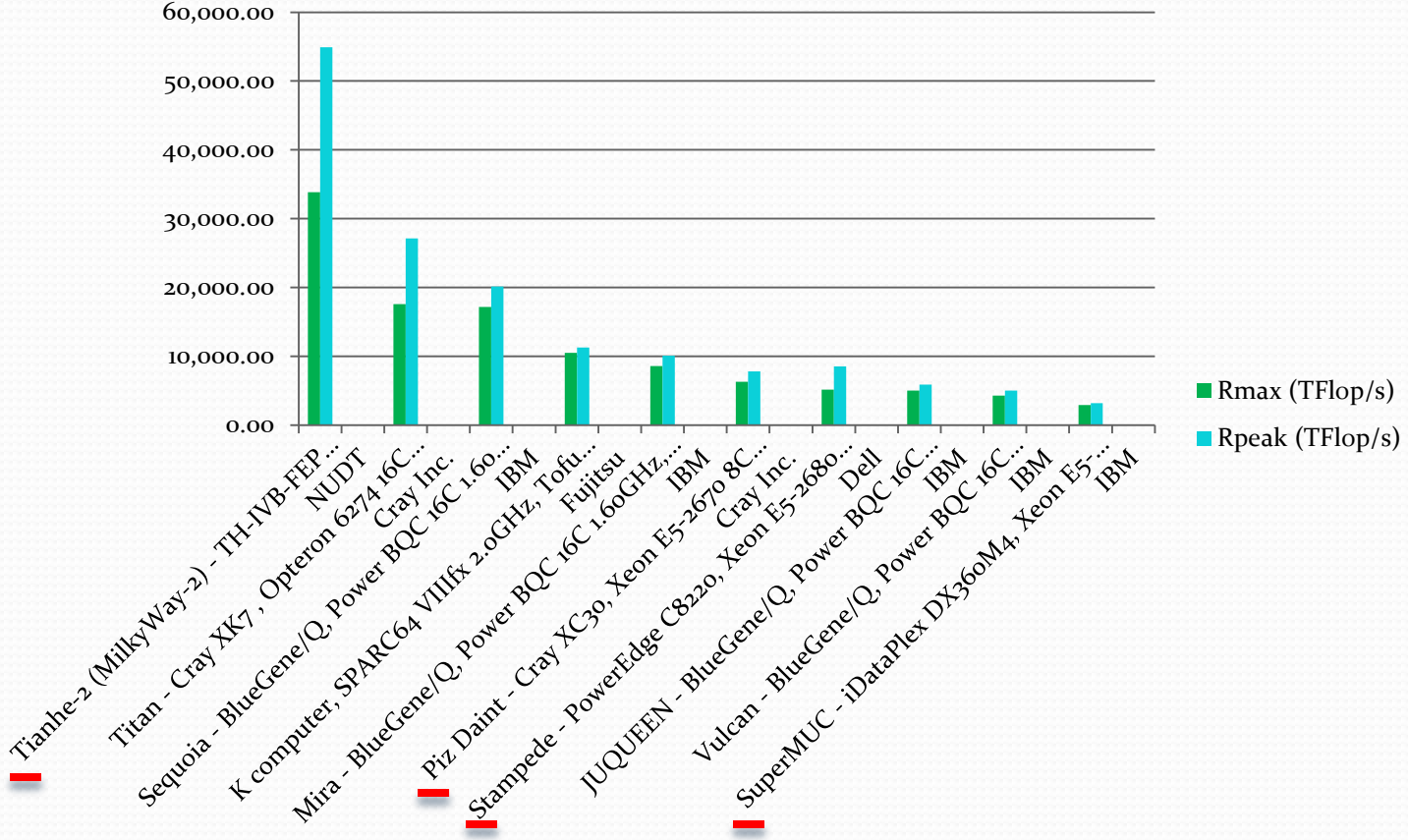
General Purpose Computing

Technical Computing

High Performance Computing

Used by 4 of the 10 fastest supercomputers (Nov. 2013)

Top 10 Comparison



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Thank You