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Vineeta Singh

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Objective: A full time position designing Digital Systems by utilizing my hands on engineering experience and strong theoretical background through education.

Availability: Immediately

EDUCATION

MSEE, Rochester Institute of Technology — August 2015

Department of Electrical and Microelectronic Engineering — GPA: 3.4/4.0

BE, University of Pune, India — June 2012

Department of Electronics and Telecommunications — GPA: 3.5/4.0

TECHNICAL SKILLS

Programming Languages	SystemVerilog, Verilog, VHDL, Matlab, Perl, Python, C, Assembly Language
Design Tools:	Xilinx ISE, Chipscope; Altera Quartus II; Cadence Custom IC Design Virtuoso Schematic, Layout, Place & Route, Spectre, PVS DRC, PVS LVS, PVS QRC, NC Verilog; Synopsys VCS, Design Compiler, DFT Compiler, PowerCompiler PrimeTime; Mentor Graphics IC Station; DevC++; Silvaco Athena Supreme; OrCAD, NI MultiSim; Diptrace; Express PCB; Eclipse
Compute Platforms:	Microsoft Windows, Linux, Apple Mac OS

EMPLOYMENT EXPERIENCE

Digital Systems I Teaching Assistant, Rochester Institute of Technology — Aug 2014 - Aug 2015

Teaching introductory digital logic & methodologies used in digital systems design for a class of 40 students. Helped students in designing and debugging projects that involve Verilog, VHDL and Gate-level Design using Altera Quartus II, Xilinx ISE, Cadence and Mentor Graphics.

Engineering Internship, Ashly Audio, Inc., Webster, NY — Jun 2014 – Aug 2014

Performed extensive prototype conformance testing and debug of professional audio quality digital signal processing products such as the Protea System Processors (4.8 SP and 3.6 SP) and Protea Signal Processors (ne24.24 M Matrix processor)

SMFL Teaching Assistant, Rochester Institute of Technology — Oct 2013- Jan 2014

Calibration and fault analysis of various semiconductor fabrication equipment in the Semiconductor and Microsystems Fabrication Lab (SMFL)

Engineering Internship, Computational Research Laboratories - TCS, Pune, India — Jun 2011- Jun 2012

Front end design of a DDR3 Memory Controller using VHDL

PROJECTS

Reliable Low-Latency and Low-Complexity Viterbi Architectures Benchmarked on ASIC and FPGA – *Graduate Research Project* — Aug 2014 – Aug 2015

In this work, different error detection schemes for architectures based on low latency, low-complexity Viterbi decoders are presented. The merit of the proposed schemes is that reliability requirements, overhead tolerance, and performance degradation limits are embedded in the structures and can be adapted accordingly. Also presented are three variants of time redundancy techniques including recomputing with encoded operands and its modifications to detect both transient and permanent faults, coupled with signature-based schemes. The instrumented decoder architecture has been subjected to extensive error detection assessments through Verilog simulations and 32nm ASIC and Xilinx Virtex 6 implementations for benchmarking.

Complex Digital System Verification — Spring 2015

Application of various concepts and technologies (Perl, Python, SystemVerilog, Verilog HDL) as related to computer architecture and complex digital system verification with an emphasis on functional verification, top down design flows and advanced methodologies.

Reconfigurable Computing Fall 2014

VHDL modeling of combinational and sequential logic for synthesis and efficient hardware implementation, architectures of modern field programmable gate arrays (FPGAs), hardware software co-design with embedded processors, hardware optimization techniques, system level integration under operating system, and dynamic reconfiguration. Projects included design and implementation of USB-FPGA communication system include UART, FIFO, Cellular RAM, programmable controller, FIR filters, and Microblaze processor implementation of the median filter in C and as a hardware accelerator of the median filter for image restoration. The final project was design and hardware Implementation of Floyd-Steinberg Halftoning Algorithm.

Design & Test of Multi-Core Chips Fall 2014

Design and implementation of logic circuits to minimize crosstalk between circuit wiring. Structures included Forbidden Overlap Code (FOC), Forbidden Transition Code (FTC), and Forbidden Pattern Code (FPC) in VHDL HLD. Performed logic design, verification, synthesis, timing analysis, and power analysis.
Design and implementation of a Network on Chip (NoC) Router/Switch in VHDL HLD. Performed logic design, verification, synthesis, timing analysis, and power analysis.

ADPCM CODEC (Encoder / Decoder) Spring 2014

This full semester class design project required high level, fixed point, bit exact software modeling, architecture development, and Top Down Design of a core level RTL database of a Multi-Channel ADPCM codec based on ITU standards G.726 and G.711 using Verilog HDL. All modules were designed, synthesized and verified at the RTL and gate level; various verification strategies were used to verify operation of the modules including directed tests coded in Verilog HDL, as well as test vectors generated by a bit exact software model of the ADPCM algorithm. Final conformance to the standards was verified using official test vectors published by the ITU. Sign-off included Static Timing closure, RTL, and ATPG coverage metrics. Including test structures, the final netlist was 1.2M gates.

16-bit Non-Pipelined & Pipelined Single-Core, RISC Processor with Assembler Spring 2014

Designed a non-pipelined and 5-stage pipelined RISC Processor with load/store architecture using Verilog RTL for processing 16-bit instructions. The Control Unit was designed in a hardwired fashion and the final database was implemented on an Altera Cyclone IV FPGA. A custom assembler was also developed in Perl for the given ISA to generate the program memory (ROM) file.

4x4 Multiplier with BIST using Mentor Graphics Fall 2013

Circuit design, simulation and characterization, layout, DRC, and LVS of a 4x4 bit multiplier including built in self test (BIST)

PMOS Inverter Fabrication Fall 2013

Semiconductor fabrication of a PMOS Inverter using processes such as oxidation, ion implantation, lithography, wet and dry etching

PUBLICATIONS

Reliable Low-Latency and Low-Complexity Viterbi Architectures Benchmarked on ASIC and FPGA (IEEE Transactions on Reliability) Aug 2015

Hand Sign Interpreter, the International Journal of Engineering and Science (IJES) Dec 2012

DDR3 SDRAM Controller, International Journal of Electronics and Computer Science Engineering Dec 2012

MEMBERSHIPS, SCHOLARSHIPS AND AWARDS

IEEE, Student Member Since 2015

Rotaract Club Shaniwarwada Pune, India, Member Since 2011

Merit Scholarship awarded by 'Tatachem Golden Jubilee Foundation' India 2013

Scholarship awarded by Sakal India Foundation 2013

2nd Prize for National Level Badminton Tournament in Zest, Pune, India 2011