Evaluation of Crosstalk Avoidance coding schemes

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***Abstract*— Propagation delay in long on-chip buses is one of the significant issues faced with respect to high-speed designs. Capacitive Crosstalk between adjacent wires on the bus increases delay as the delay of the wire is dependent on the electrical state of its neighboring wire and transitions of signals. It can trigger timing violations and also cause more power dissipation. The problem becomes acute for long on-chip buses which are responsible for the basic operations of NoC infrastructures utilized as part of the communication infrastructure of large Multi Processor SoCs (MP-SoCs).**

Shielding can be used by placing a grounded wire between each signal wire which helps in alleviating the crosstalk problem but doubles the area required by the bus. Crosstalk avoidance codes (CAC) can be employed to minimize crosstalk delay and reduce energy dissipation in NoC data streams. CAC helps in reducing the coupling capacitance and improving the signal integrity. In this paper, we present an implementation of Forbidden Pattern Condition (FPC), Forbidden Transition Condition (FTC), Forbidden Overlap Condition (FOC) schemes by using encoder-decoder circuits for a 90nm process.

***Index Terms*—Crosstalk Avoidance codes, FOC, FTC, FPC, Encoder, Decoder, NoC, bus, area, power, energy.**

I. INTRODUCTION

The network-on-Chip (NoC) improves the integration of large numbers of computational and storage blocks in a single chip. The communication between the functional blocks takes place with the help of switches and global on-chip buses. The on-chip global buses face the issue of large propagation delays with increase in their lengths. In the deep sub-micron (DSM) era, due to routing density, inter-wire spacing is reduced which gives increases in coupling capacitance between neighboring wires [1]. The coupling capacitance between the wires is responsible for delay through a long wire. The Miller Effect (also know as Miller Coupling Factor or MCF) where the transition takes place in opposite direction for the neighboring wires has a more adverse effect on the delay. When cross-coupling capacitance exceeds the loading capacitance on the wires, the delay observed for such a transition may be equal to or greater than twice that of a wire transition adjacent to a steady signal. This kind of delay can be termed as "crosstalk delay" [2].

Crosstalk delay becomes an issue in the communication fabrics of NoC as it can cause some timing violations, and cause more power dissipation. Power consumption and energy dissipation is an important concern with respect to multi-core SoC design. For some high-speed designs, crosstalk delay limits the clock speed. Crosstalk can be reduced by using shielding which in one scheme involves placing a grounded wire between every pair of signal wires. Although it helps in eliminating the crosstalk within the bus, it doubles the wiring area. In NoC domain, cross-chip buses are often required to be routed in higher metal layers which are scaled slower compared to the rest of the layers for preventing an unacceptable increase in resistance. Thus it is unacceptable to justify doubling the bus width as the routing resources are already scarce. Coding techniques can be used to avoid crosstalk delay.

Coding can be explained as the process of mapping information bits or the incoming data words into code-words that exhibit certain desired properties. The values which are placed by the encoder on the channel are called as code-words. Different coding schemes have been proposed to reduce power consumption of on-chip buses. In order to prevent crosstalk delay, any two adjacent code-words should not have transitions which may incur crosstalk delay [3]. As crosstalk is data dependent, different coding schemes aim to reduce the amount of relative transitions between adjacent wires. Thus the effective switching capacitance increases the speed of the signal transmission by reducing effective switching capacitance. The FOC, FTC, and FPC coding schemes have been implemented for bus-based systems. Crosstalk avoidance

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coding schemes can be used to reduce the coupling capacitance thereby enhancing system reliability and at the same time reducing communication energy as it avoids doubling the number of wires. This helps in reducing the overall energy dissipation. CACs help in reducing the worst-case switching capacitance by ensuring that the transition from one to the other code-words does not cause the wire to switch in opposite directions.

In this paper, we discuss three types of crosstalk avoidance codes which achieve different degrees of delay reduction. The HDL model for the encoder and decoder of the three models has been simulated and synthesized using the 90nm technology library. Some analytical calculations have been performed on the un-coded and coded wires using the synthesis results to calculate the total wire capacitance.

The organization of the paper is as follows: In Section II, the bus models have been explained. In Section III, the three popular crosstalk avoidance codes have been discussed. In Section IV, the simulation and implementation results of the encoder and decoder models of FTC, FPC, and FOC are discussed and it also contains the analytical calculations based on the synthesis results. Finally, the conclusions are made in Section V.

II. SoC Physical Design Issues

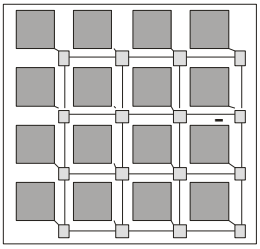


Figure.1 Mesh-based NoC

For NoC interconnect architectures, the communication between processor cores takes place by using switches and links. Data exchange between functional blocks is carried out using packets.

The delay of the wire is dependent on transitions in the wire and those adjacent to it. The worst case delay of the wire is given as (1+4 λ) τ, where τ represents the delay of the wire free from crosstalk and λ represents ratio of coupling capacitance to bulk capacitance.

A. Bus Models- Delay Model

The analytical model for delay in DSM buses is discussed in the following. Assumption of n-bit parallel bus in a single metal layer has been formed. The rise time of the drivers as well as the interconnect losses such as inductance can be ignored. These DSM buses can be modeled as distributed RC networks consisting of coupling capacitances between the adjacent wires [3]. The delay of a line *l (1 < l < n)* of the bus is given by [4]:

$$T_l = \tau_0 [(1 + 2\lambda)\Delta_l^2 - \lambda\Delta_l(\Delta_{l-1} + \Delta_{l+1})] \quad (1)$$

Where τ is delay of a line free from crosstalk, λ is ratio of coupling capacitance to bulk capacitance. The model shows that the delay of a line is dependent on the transitions happening in the adjacent lines.

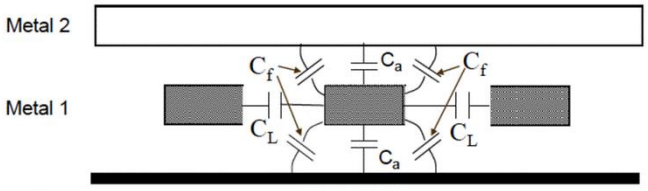


Figure.1 Types of capacitances

Total Capacitance can be defined as

$C_{total} = C_{area} + C_{lateral} + C_{fringe}$

Area capacitance can be calculated as

$C_a = (\varepsilon_{ox}.W)/H = 0.035$ fF/um (W/H)

H represents the spacing between the two metal layers, and W represents the width of interconnect.

Lateral capacitance can be calculated as

$C_L = (\varepsilon_{ox}.T)/S = 0.035$ fF/um (T/S)

The lateral capacitance is the coupling capacitance between interconnects, T is the thickness, and S is the spacing.

Fringe capacitance for widely spaced conductors is given as

$C_{fringe} = \varepsilon_{ox}.\ln(1 + T/H)$

When the neighboring wires experience transitions, the coupling capacitance depends on those transitions. Cc represents the lateral capacitance.

Table.1 Coupling Capacitance on Victim

Conditions	Victim Capacitance
victim and aggressors switch in the same direction	$C_{victim} = C_{area}$
victim and one aggressor switch in the same direction and the other aggressor remains quiet	$C_{victim} = C_{area} + C_C$
victim switches and both aggressors are quiet	$C_{victim} = C_{area} + 2C_C$
victim and 1 aggressor switch oppositely, while the other aggressor is quiet	$C_{victim} = C_{area} + 3C_C$
victim and both aggressors switch oppositely	$C_{victim} = C_{area} + 4C_C$

III. CROSSTALK AVOIDANCE CODING (CACS)

A) Forbidden Overlap Codes (FOC)

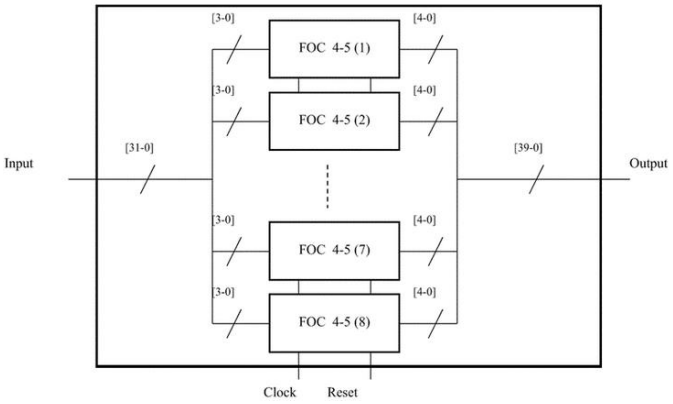
The worst-case delay in wire $(1+ 4\lambda)\ \tau$ occurs in a wire when there is one rising (falling) transition on it and falling (rising) transition on the neighboring wires. For satisfying this condition, the transition of the code-word from 010 to 101 cannot be made. Forbidden Overlap Code (FOC) meets this criterion. One simple way to achieve the forbidden overlap condition is to use half-shielding, where one ground wire follows two signal wires. The disadvantage of using that method is the requirement of extra wires. Hence encoding the data links is one preferred way to satisfy the condition. Considering practical limitations such as size and complexity of codec hardware, it is not possible to do the encoding for all the data bits. However the links are divided into sub-channels and are encoded using CACs, and then those sub-channels can be combined in a way that crosstalk can be avoided.

Table 2: Coding scheme of FOC_{4-5}

Data bits				Code bits				
d3	d2	d1	d0	c4	c3	c2	c1	c0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	0	0	1
0	0	1	1	0	0	1	0	1
0	1	0	0	0	0	0	1	1
0	1	0	1	0	0	1	1	1
0	1	1	0	1	0	0	1	1
0	1	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0	0
1	0	0	1	1	0	1	0	0
1	0	1	0	1	0	0	0	1
1	0	1	1	1	0	1	0	1
1	1	0	0	1	1	0	0	0
1	1	0	1	1	1	1	0	0
1	1	1	0	1	1	0	0	1
1	1	1	1	1	1	1	0	1

For the design of 32-bit inputs FOC, eight FOC (4-5) blocks are required and thus a 32-bit un-coded wire gets converted into a 40-bit coded wire. The two sub-channels do not require any shielding when they are placed next to each other for the forbidden overlap condition. For FOC, the maximum coupling factor can be reduced to p = 3.

Figure 2: FOC_{32-40} Block Diagram using $FOC4_{-5}$



B) Forbidden Transition Codes (FTC)

The transitions between the successive codes should not cause the neighboring wires to switch in opposite directions like a code-word cannot switch from 01 to 10 bit pattern and from 10 to 01. This is the Forbidden Transition Condition. Thus by extending some non-permissible transitions, the maximum capacitive coupling and maximum delay can be reduced further as compared to FOC. The maximum coupling factor for FTC can be reduced to p = 2. The codes satisfying this condition are called as Forbidden Transition Codes (FTC). The simplest FTC can be realized by employing the design where a shielding wire is inserted after each signal line. For building wider links, the inter-switch links are divided into sub-channels and they are encoded separately. Thus hierarchical encoding is preferred. It has to be noted that the sub channels need to be combined such that there should be no forbidden transition at the boundaries.

For the design of a 32-bit input FTC, eleven FTC (3-4) blocks are needed and thus a 33-bit input (where one additional 0 is added) gets converted into a 44-bit coded wire.

Table 3: FTC_{3-4} Coding scheme

Data bits			Code bits			
d2	d1	d0	c3	c2	c1	c0
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	0	1
0	1	1	0	1	0	1
1	0	0	0	1	1	1
1	0	1	1	1	0	0
1	1	0	1	1	0	1
1	1	1	1	1	1	1

C) Forbidden Pattern Code (FPC)

The coupling factor for FTC is also p = 2. It is possible by avoiding 010 and 101 bit patterns for the code words. This condition is called as FPC. The simplest FPC can be made by incorporating duplication where bits are sent using two neighboring wires. When the sub-channels are combined, the boundaries need to be checked for forbidden pattern conditions.

For the general consideration, after coding and decoding techniques are applied for executing CACs, if the un-coded wire is considered to have n signal lines, and the coded wire has k > n wires, the code can be called as a (n, k) code.

For implementing the $FPC_{32\text{-}40}$ encoder, eight $FPC_{4\text{-}5}$ are combined together.

Table 4: Coding scheme for $FPC_{4\text{-}5}$

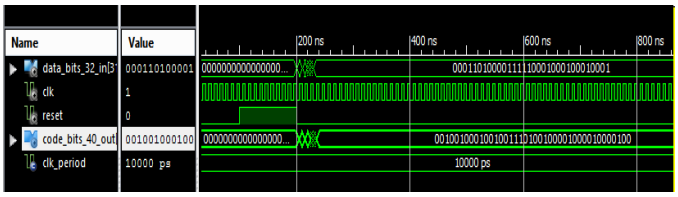
Data bits				Code bits				
d3	d2	d1	d0	c4	c3	c2	c1	c0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	1	1	0
0	0	1	1	0	0	0	1	1
0	1	0	0	0	1	1	0	0
0	1	0	1	0	0	1	1	1
0	1	1	0	0	1	1	1	0
0	1	1	1	0	1	1	1	1
1	0	0	0	1	0	0	0	0
1	0	0	1	1	0	0	0	1
1	0	1	0	1	1	0	0	0
1	0	1	1	1	0	0	1	1
1	1	0	0	1	1	1	0	0
1	1	0	1	1	1	0	0	1
1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	1	1

IV. SIMULATION AND IMPLEMENTATION RESULTS

A) SIMULATION RESULTS-

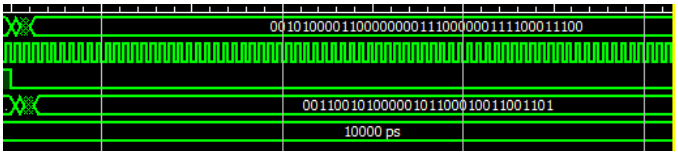
VHDL was used to write the models for the CACs which helps to describe the working of a logic circuit. After the logic has been written, the design has been tested by writing a separate test-bench for each of the individual files. The test-bench helps in verifying whether or not the code is working the way it should be. By performing gate-level simulation, the timing constraints of the code can be viewed in great detail as it takes propagation delay into account.

FOC Encoder results-



For the FOC encoder, it can be seen that for the given input data-word of 32 bit '00011010000111110001000100010001', the output '00100100010010011101001000010000100000100' is obtained which is perfect for the FOC encoder.

FOC Decoder Results-



The decoder operates in the reverse way of the encoder, and thus for 40-bit input code-word '00101000011000000001110000001111000011100', the output data-word obtained is '00110010100000101100010011001101' which matches the expected results for the FOC decoder.

Similarly, the waveforms for FTC encoder-decoder, and FPC encoder-decoder are verified. This has been achieved by writing one VHDL file for FOC encoder (4,5) and one for FOC decoder (5,4) and then instantiating them eight times in their top files i.e FOC encoder (32, 40) and FOC decoder (40, 32). FPC has been implemented in similar way. For FTC, the FTC encoder (3, 4) and FTC decoder (4, 3) has been written and simulated, and these files are instantiated eleven times in the top files.

B) SYNTHESIS RESULTS-

The design has been synthesized using the Design Vision Synopsys tool. TSMC 90nm technology library was used to set the path. The synthesis reports helped in generating the experimental results. The power, are, and timing reports for each of the three encoders and decoders have been generated. Power dissipation for encoder and decoders for all the schemes are shown below.

Table 5: Area coverage and Power dissipations for FOC

FOC Module	Power in watts	Area in $(um)^2$	Total area $(um)^2$
Encoder	1.34E-04	2340.1	4497.8
Decoder	7.52E-05	2154.7	

Table 6: Area coverage and power dissipation in FPC

FPC Module	Power in watts	Area in $(um)^2$	Total area $(um)^2$
Encoder	7.91E-05	3329.5	5797.8
Decoder	6.21E-05	2468.3	

Table 7: Area coverage and power dissipation in FTC

FTC Module	Power in watts	Area in $(um)^2$	Total area $(um)^2$
Encoder	8.46E-05	3467.5	6121.6
Decoder	8.78E-05	2654.1	

Table 8: Delay comparison of CACs

Module	Delay (PS)	Total Delay (PS)
FOC Encoder	1.1	
FOC Decoder	421.8	422.9
FPC Encoder	237.8	
FPC Decoder	311.9	549.7
FTC Encoder	298.6	
FTC Decoder	423.75	722.35

From the timing values obtained from the reports, it can be observed that FTC encoders and decoders have highest power dissipation and highest delay of all the three schemes.

The analytical model for the un-coded and coded bus has been developed. The assumption that all wires are on metal 2 is made for the calculations.

For power and energy calculations,

$$E = \alpha * C * V_{dd}^2$$

$$P = E * f$$

In order to carry out the calculations for un-coded wire, the length is varied. FPC has the highest energy dissipation values.

Table 9: Power dissipation and energy for un-coded wires

Length (mm)	Power (watt)	Energy (Joules)
1	1.70E-02	1.02E-11
2	3.38E-02	2.03E-11
3	5.07E-02	3.03E-11
4	6.75E-02	4.04E-11
5	8.43E-02	5.05E-11
6	1.01E-01	6.06E-11
7	1.18E-01	7.06E-11
8	1.35E-01	8.07E-11
9	1.52E-01	9.08E-11
10	1.68E-01	1.01E-10

Table 10: Power dissipation and energy for FOC

Length (mm)	Power (watt)	Energy (Joules)
1	1.17E-02	7.02E-12
2	2.33E-02	1.39E-11
3	3.49E-02	2.09E-11
4	4.64E-02	2.78E-11
5	5.80E-02	3.47E-11
6	6.96E-02	4.16E-11
7	8.11E-02	4.86E-11
8	9.27E-02	5.55E-11
9	1.04E-01	6.24E-11
10	1.16E-01	6.93E-11

Table 11: Power dissipation and energy for FPC

Length (mm)	Power (watt)	Energy (Joules)
1	1.83E-02	1.09E-11
2	3.64E-02	2.18E-11
3	5.45E-02	3.26E-11
4	7.26E-02	4.35E-11
5	9.07E-02	5.43E-11
6	1.09E-01	6.51E-11
7	1.27E-01	7.60E-11
8	1.45E-01	8.68E-11
9	1.63E-01	9.77E-11
10	1.81E-01	1.09E-10

Table 12: Power dissipation and energy for FOC

Length (mm)	Power (watt)	Energy (Joules)
1	2.337E-02	2.80E-11
2	4.674E-02	2.80E-11
3	7.011E-02	4.20E-11
4	9.35E-02	5.60E-11
5	1.17E-01	7.00E-11
6	1.40E-01	8.40E-11
7	1.64E-01	9.80E-11
8	1.87E-01	1.12E-10
9	2.10E-01	1.26E-10
10	2.34E-01	1.40E-10

Critical length plays a major role as encoding schemes are of no use for lengths below it. It has been calculated by putting in different values and finding out the lowest amongst all.

It can be observed that FTC appears to have the least critical path.

Table 12: Critical length of encoded bus

CAC scheme	Length(mm)
FOC	0.03156
FPC	0.029
FTC	0.0145

V. CONCLUSION

Network on chip is one promising emerging field as it helps to integrate numerous cores in single SoC. In order to have a widespread adoption of NoC paradigm, system reliability issues needs to be addressed.

Crosstalk between adjacent wires is becoming a major issue in the deep sub-micron IC design. Crosstalk avoidance codes (CACs) help to mitigate the problem of crosstalk delay on the buses. It helps to reduce the coupling capacitance of the wire segments and thus plays an important role in reducing the energy dissipated in the communication fabric.

In this paper, the energy and power dissipation for an un-coded 32 bit bus was discussed and the results were compared with the energy dissipation of CAC schemes like FTC, FOC and FPC.

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